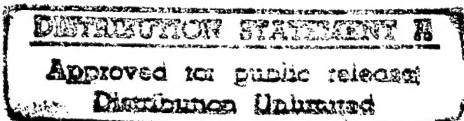Progress Report

Giant Magnetoresistive Sensors
A Phase II SBIR
Contract N00012-96C-0342

To

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Office of Naval Research

From

Nonvolatile Electronics, Inc.
11409 Valley View Road
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Progress Report

Giant Magnetoresistive Sensors
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1) Program Overview

This report covers primarily the period from May 15, 1997 to July 25, 1997 - from month 10 through month 11 and into month 12 of the program. This period has concentrated on fabricating tunneling bridge sensors with on-chip bias coils, developing the test equipment needed to test sensors at 10^{-8} Gauss, and developing a drive/sense scheme which can be used to overcome the effects of 1/f noise. As we near the end of the first year of the program, pinned tunneling sensors are in process which will be used to make a hybrid circuit (breadboard) version of the sensor.

A test system for measuring sensors down to 10^{-8} Gauss is nearly completed. A clear plastic fixture with 3 axis coils has been completed. The design of the electronics is complete, board assemblies have been ordered, and assembly has begun. The system will be completed by the first week in August.

An AC drive/sense scheme was developed to reduce the effects of 1/f noise. A GMR sandwich sensor bridge was used for the experiment. Magnetic noise due to domain motion at low fields was not expected to be reduced by this technique, and it wasn't. However, the scheme was successfully tested and should work when used for the biased tunneling sensor.

The sensor bridge design described in the May report was fabricated, and included the successful integration of bias coils. Some difficulties were encountered with maintaining adhesion of metal and dielectric layers, and in retaining spin dependence of the tunneling currents.

Spin tunneling sensors have been designed and processed in this first year of the program. The fundamental signal-to-noise ratio of a pinned tunneling device was shown to be within a factor of ten of the program goal, and the chances of reaching the goal appear to be good. The use of pinned tunneling junctions with hard direction biasing appears at this time to be a good program decision. The vertical profile of the process has become more complex as a result, and this has resulted in some process difficulties, particularly in the areas of defining iron manganese pinning layers (iron manganese is a highly reactive material), and with trying the idea of making two types of cobalt-ruthenium-cobalt sandwiches in a bridge in order to get opposite pinning in opposite legs of the bridge. The iron manganese layers are now ion milled successfully, and an improved

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material (iridium manganese) will be tried in the second year. No fundamental problems have been encountered with the two cobalt-ruthenium-cobalt sandwiches, but the addition of a photo masking step and a back-sputter step has complicated the process somewhat, and some process development remains. It is expected that reproducible results will be achieved on these more complex processes in the next 6 months.

In the second year of the program, the primary goal is to integrate the bridge with integrated circuits, and to establish sensor capabilities down to 10^{-8} Gauss. In the next 6 months we will establish compatibility with integrated circuits, and we intend to explore both linear bipolar and CMOS compatibility. The first step is to establish the thermal endurance of the spin tunneling devices, work which has already begun. Linear bipolar circuits are less sensitive to radiation damage, and require only 150-200 C annealing temperatures. CMOS requires about 250 C for annealing. If the tunneling devices cannot withstand 250 degrees for two hours, we will concentrate on linear bipolar underlayers.

Another technical issue is the trade-off between using a second coil on chip versus using a bias magnet in the package or an external coil. An experiment where neodymium iron boron powder was embedded in the molding material of the IC package was encouraging. A 5 Gauss bias was established which should be stable to 1000 Gauss external fields (the powder has >10,000 Gauss coercivity). If the bias can be controlled at about 20 Gauss, it would be a desirable solution because it requires no power. A second set of on-chip bias coils or external windings are back-up solutions. The in-package bias technique will be explored more fully in the next six months.

The last 6 months of the current program (integrated single axis 10^{-8} Gauss sensor demonstration) will incorporate the next six month's results and be dedicated to the design, build, and test of the sensor. The integrated circuit design will be a minor variation of an existing linear amplifier design, but a new mask set and a lot of foundry wafers will be needed.

The remainder of this report is devoted to a description of the low field test setup (coils and electronics design), circuit drive and sense techniques to reduce the effect of 1/f noise, and processing bridge sensors with integrated coils.

2) Test apparatus design

In the last quarter, our three-axis Helmholtz coil arrangement has been assembled. The fundamental properties of this apparatus were described in the last report. The main result is that we now have complete capacity to control the size and orientation of magnetic fields required for testing a pT sensor. Pictures of these coils are shown below.
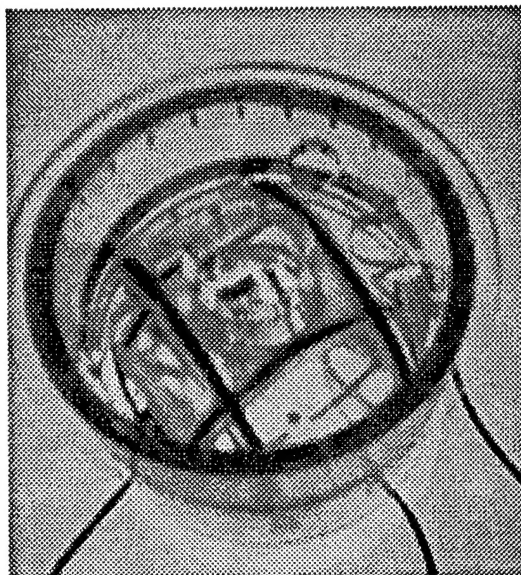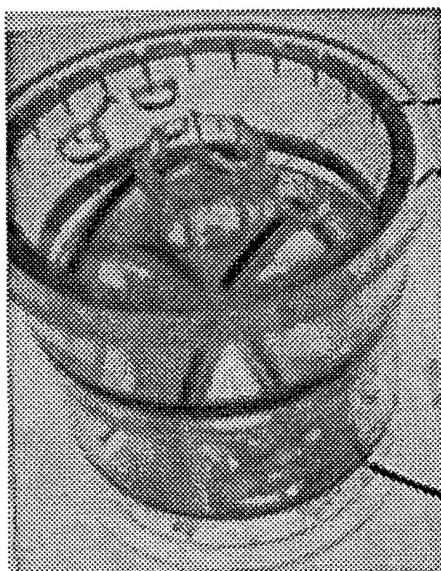

Figure 1:   The coils are made out of clear acrylic tubing. A sample stage is attached to the lid and extends down to the active region of the coil arrangement. The lid has three finger holes for easy handling and extra wire passage.

What may be not obvious from the pictures is that the coils for each axis are actually three sets of coils. These coils were wound professionally at Nicollet Technology to ensure a uniform winding. The first set has one turn, the second has 25 turns, and the third has 250 turns. This gives us the ability to test many biasing, excitation, and feedback methods. The coils are large enough so that there is a region of pT uniformity several mm on a side.

3) AC excitation and demodulation technique

An AC excitation circuit has been designed and constructed on a printed circuit board. Pictures of the board and circuit diagrams are shown in Figure 2.
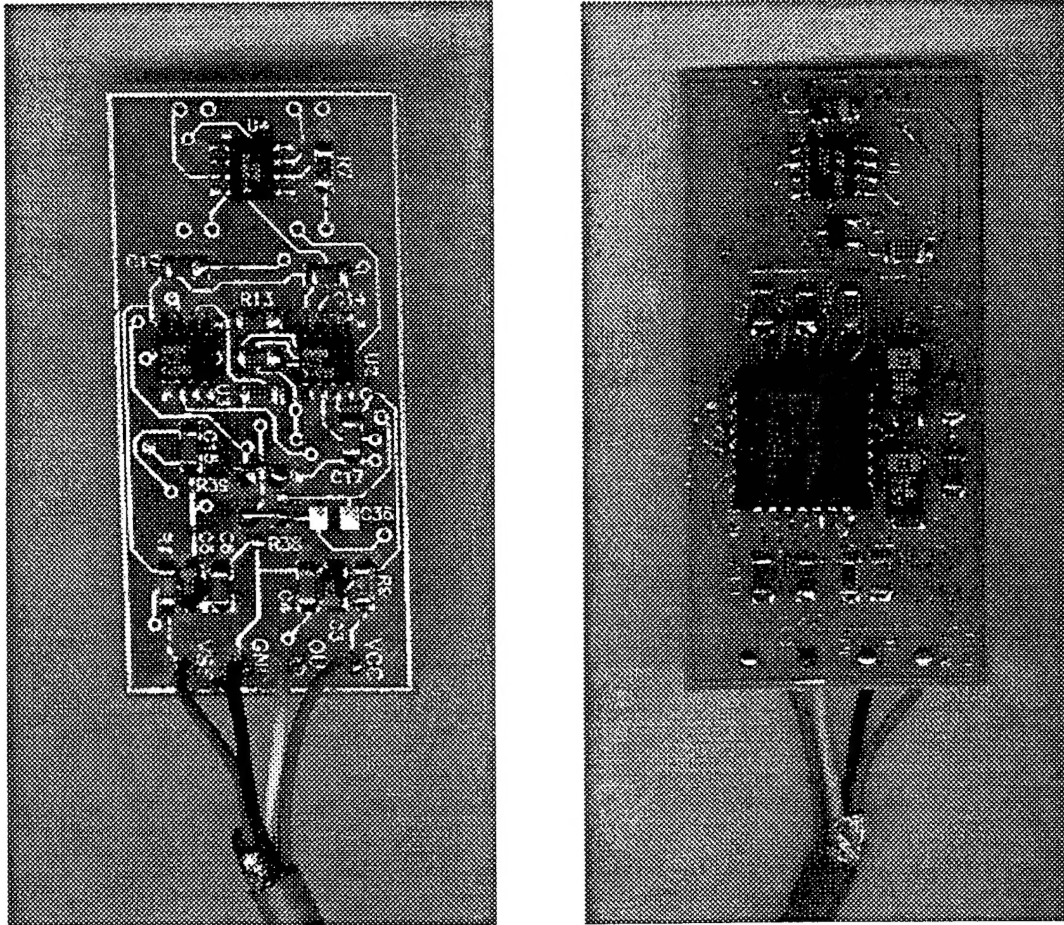
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Figure 2:   The front and back of our AC sensor excitation board.

The purpose of this circuit is to improve the signal to noise ratio of the basic bridge sensor. Based on previous experience, it is expected that a factor of ten improvement is achievable with this type of circuitry. There is some question, however, whether the improvement will be as significant at low frequencies with magnetic sensors.

There are several modes of operation being tested. They are: 1) AC bridge current excitation mode, 2) AC field biasing, 3) AC bridge excitation on a DC offset, and 4) a combination of AC field biasing and bridge excitation. All of these modes are designed to generate an AC sensor bridge output which can be demodulated with a synchronous reference signal. Some data have already been collected using the first mode with sensor bridges made of GMR material, and this is the preferred mode for second year of the program. Schematics of operating modes are shown below in Figures 3 and 4.
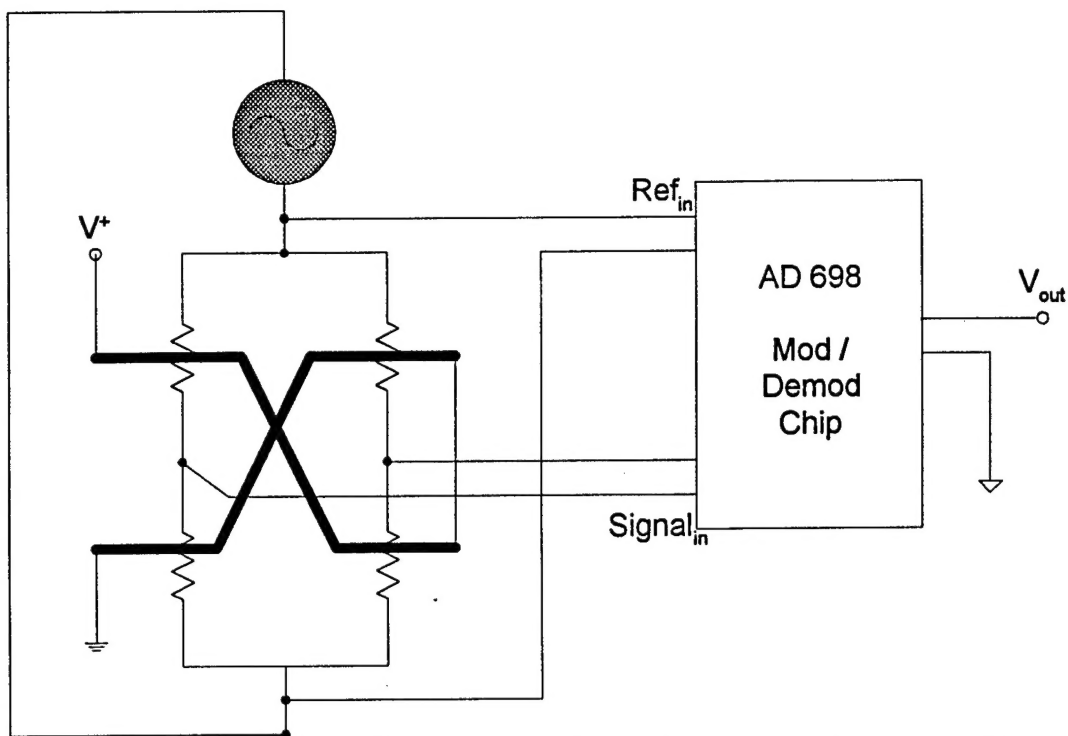
Figure 3: AC mode #1. The magnetoresistive bridge is excited by an AC current. The bias straps, in red, carry a DC current which provides a DC field bias to the magnetoresistors. The actual circuit diagram is shown in Figure 4.
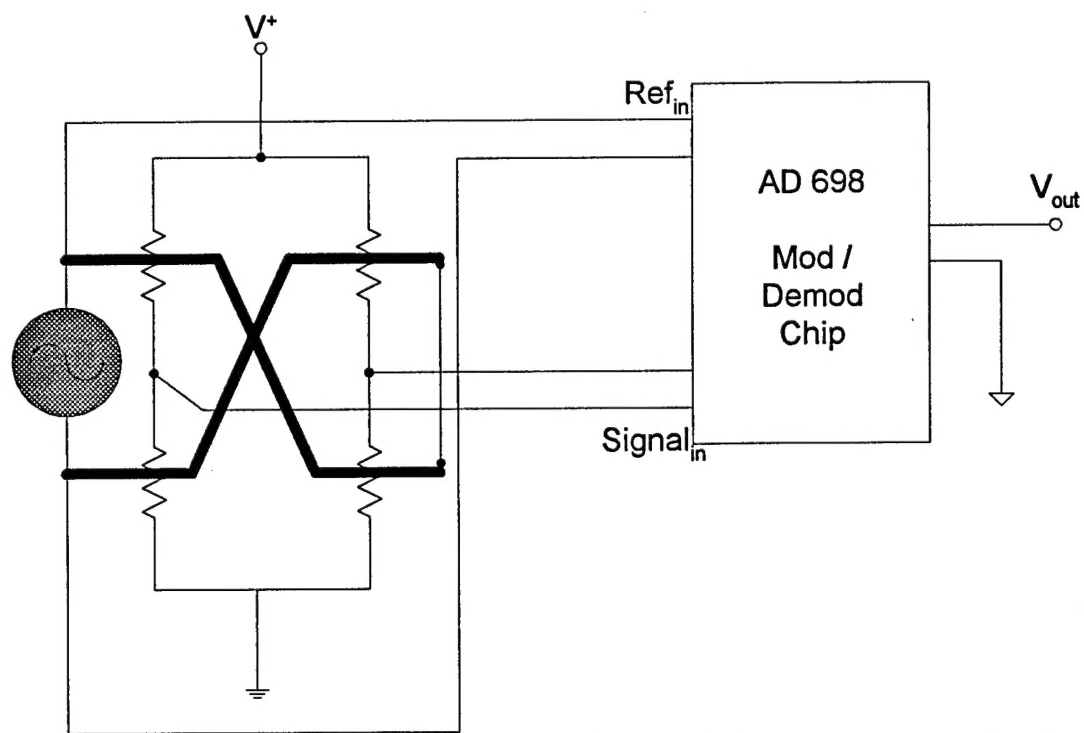

Figure 4: AC mode #2. The magnetoresistive bridge is excited by an DC current. The bias straps, in red, carry an AC current which provides an AC field bias to the magnetoresistors.
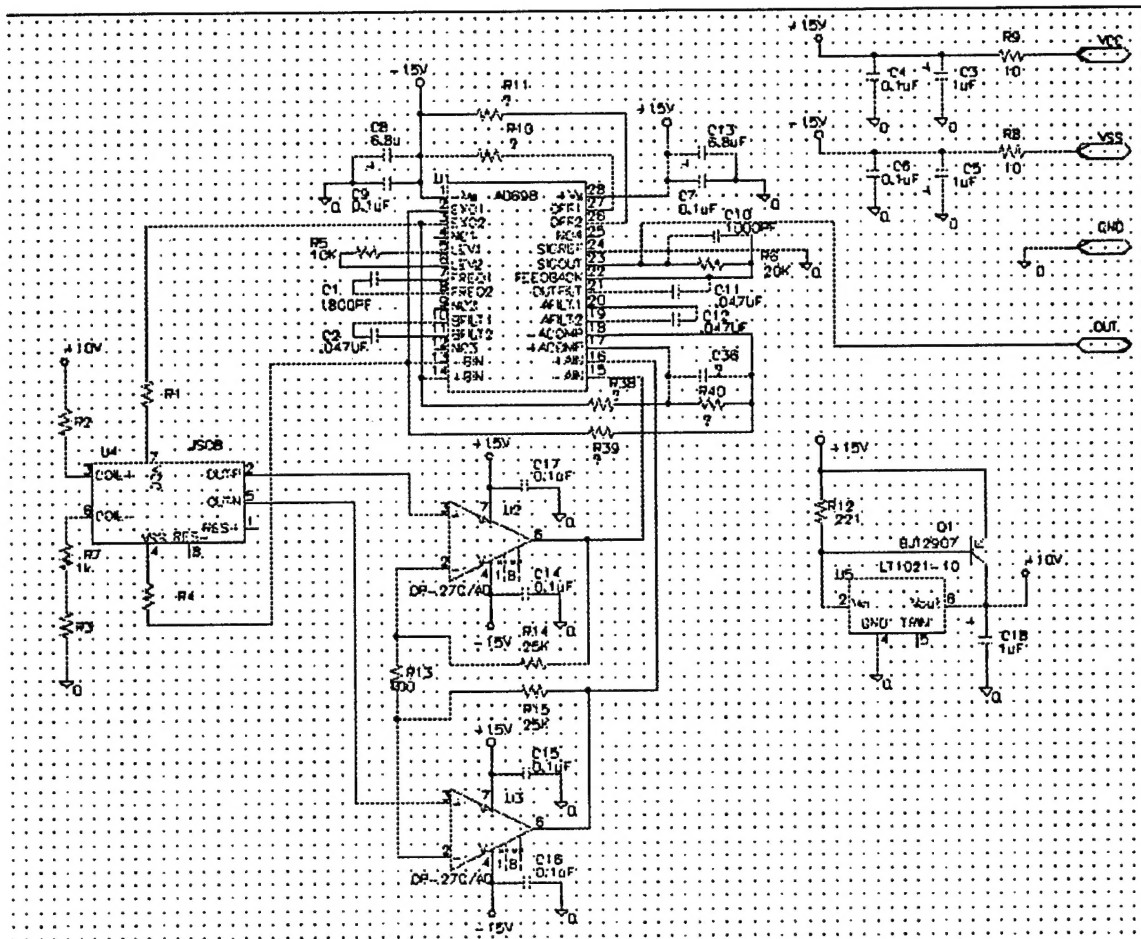
Figure 5: The circuit diagram for the AC breadboard.

So far, only mode #1 (see Figure 3) has been tested extensively. This mode shows some promise. Noise measurements using a spectrum analyzer show a noise level of about 500 µV/root Hz from a standard GMR sensor. This corresponds to a field of 0.25 mOe. Pictures of the spectrum analyzer output is shown in Figure 6.

We expect that this AC mode will reduce 1/f noise in the SDT sensors. Since there are many variables to adjust in designing this type of circuit, we are constructing a more modular test system based on the original circuit shown above. This will allow easy changes of critical parameters such as drive frequency and amplitude, input amplifier gain and bandwidth, phase shift, and output amplitude. This system uses low noise mini-mic jacks, all cabling is through shielded twisted pairs, and extra care is taken with grounding and shielding issues.
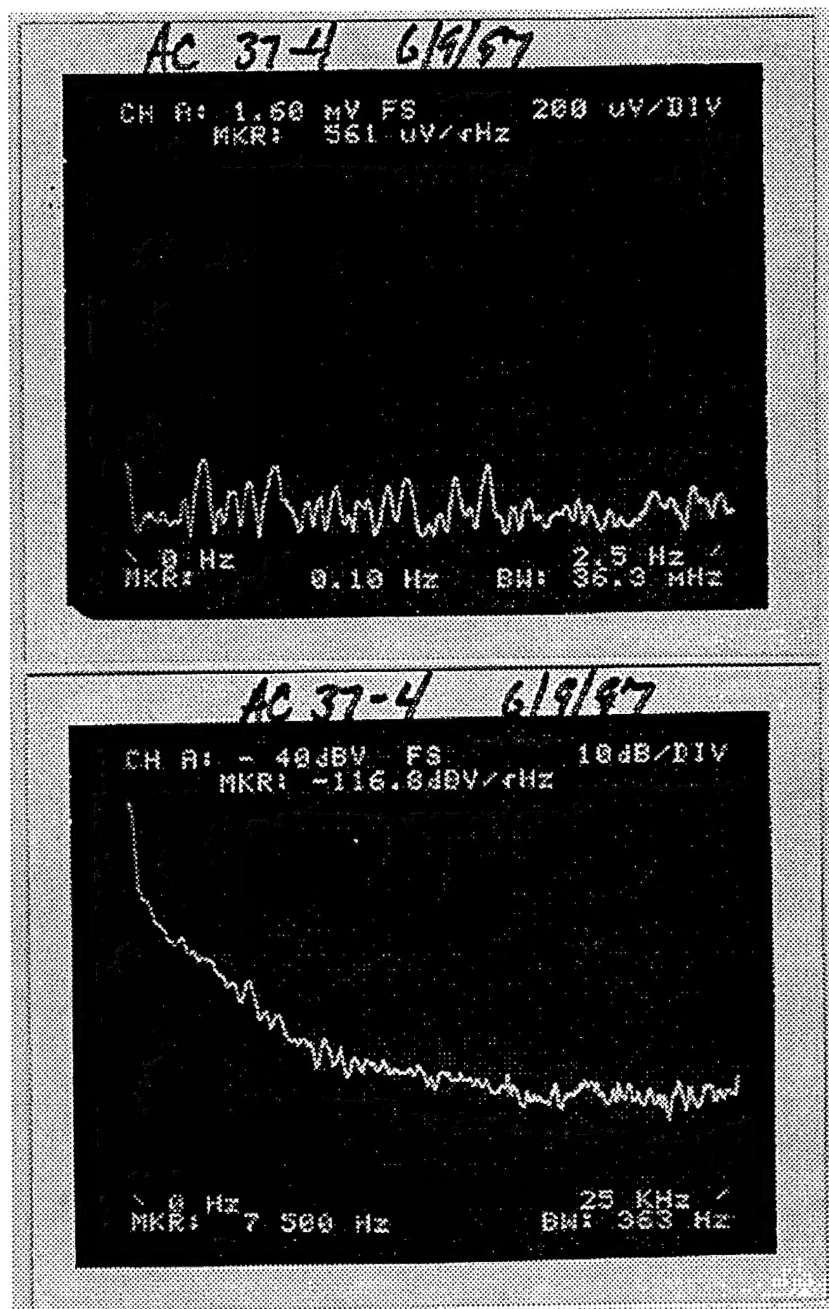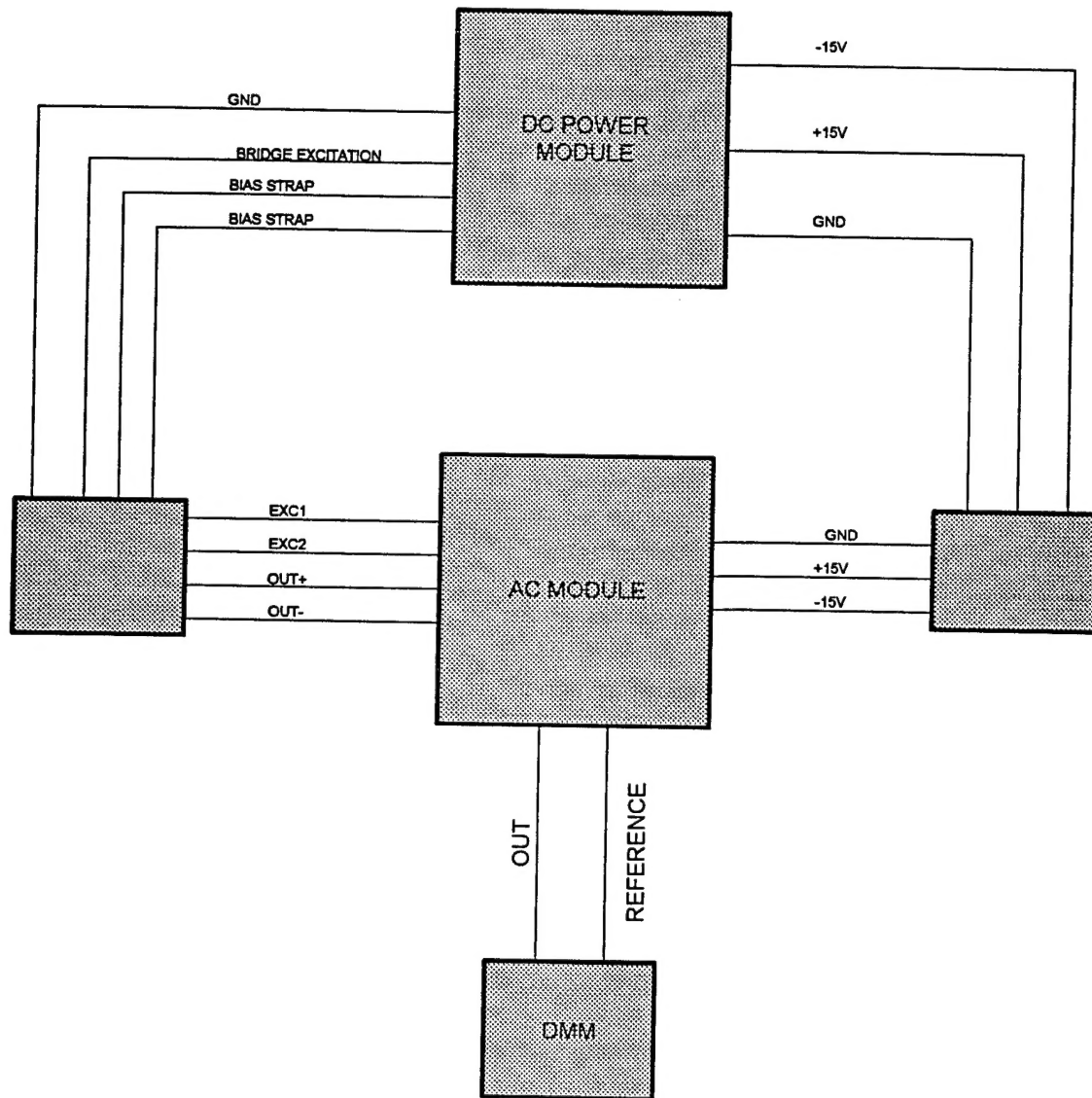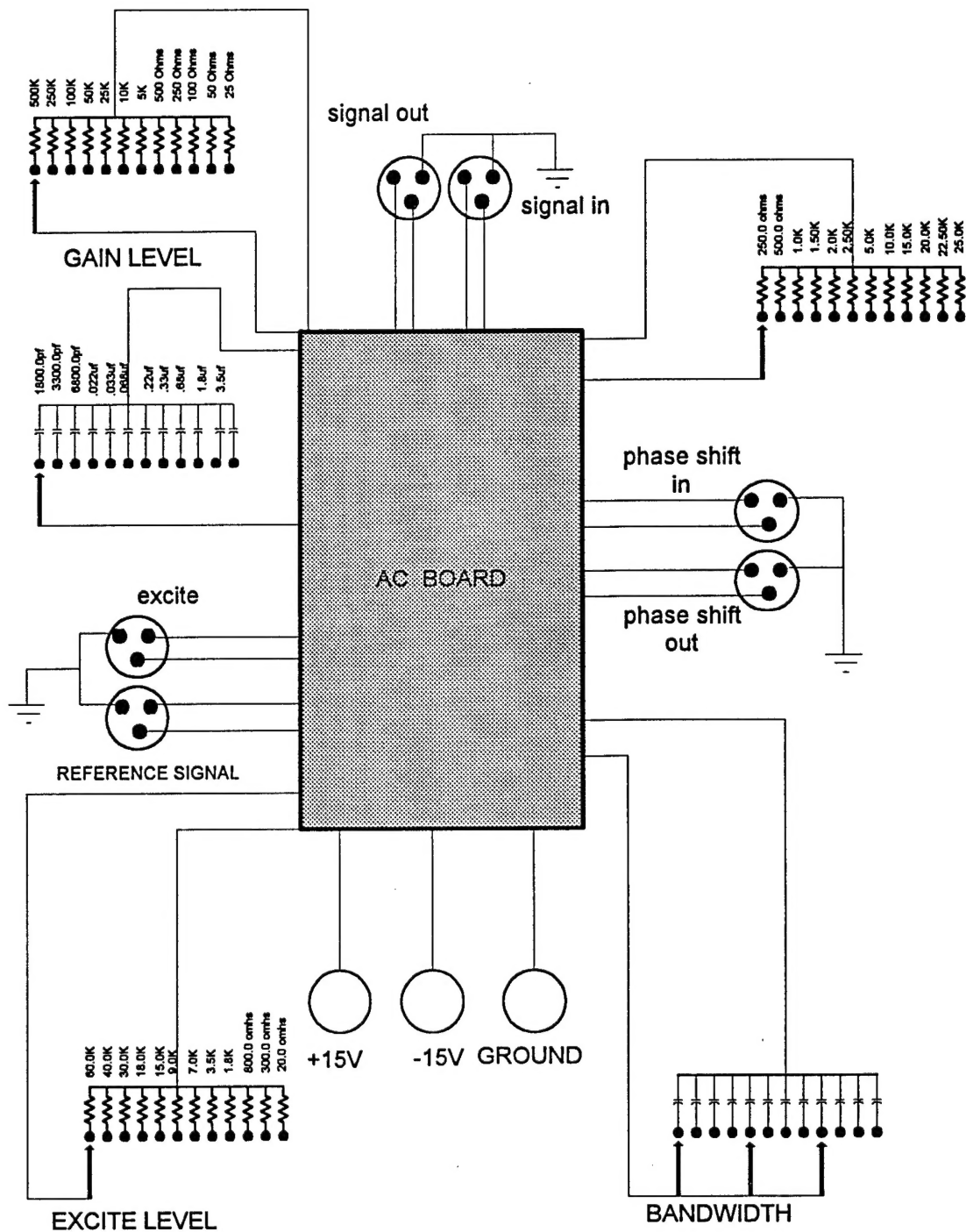
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Figure 6: Spectrum analyzer output for the AC current excited bridge. The top picture shows a 0 to 2.5 Hz range while the bottom picture shows a 0 to 25 kHz range.

Improving our noise measurements has been a major focus in the past two months. We have succeeded in measuring the Johnson noise of a 100kΩ special low noise resistor to within 5% of the expected value (40 nV/rt. Hz). This gives us a high confidence with the measurements we are making on tunneling devices.

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DC POWER MODULE

-15V

GND

+15V

BRIDGE EXCITATION

BIAS STRAP

BIAS STRAP

GND

EXC1

EXC2

OUT+

OUT-

AC MODULE

GND

+15V

-15V

OUT

REFERENCE

DMM

SYSTEM BLOCK DIAGRAM

Figure 7: The low field test electronics are shown here schematically. The AC and DC modules are shown in more detail in the next several diagrams. This system makes for easy testing of many sensor schemes.

GAIN LEVEL

500K 250K 100K 50K 25K 10K 5K 500 Ohms 250 Ohms 100 Ohms 50 Ohms 25 Ohms

signal out

signal in

250.0 ohms 500.0 ohms 1.0K 1.50K 2.0K 2.50K 5.0K 10.0K 15.0K 20.0K 22.50K 25.0K

1800.0pf 3300.0pf 6800.0pf .022uf .033uf .068uf .22uf .33uf .68uf 1.8uf 3.5uf

AC BOARD

phase shift in

phase shift out

excite

REFERENCE SIGNAL

60.0K 40.0K 30.0K 18.0K 15.0K 9.0K 7.0K 3.5K 1.8K 800.0 ohms 300.0 ohms 20.0 ohms

+15V   -15V   GROUND

EXCITE LEVEL

BANDWIDTH

AC MODULE BLOCK DIAGRAM

Figure 8: The AC module provides for a variety of excitation levels, phase shifts, bandwidths, and gains.
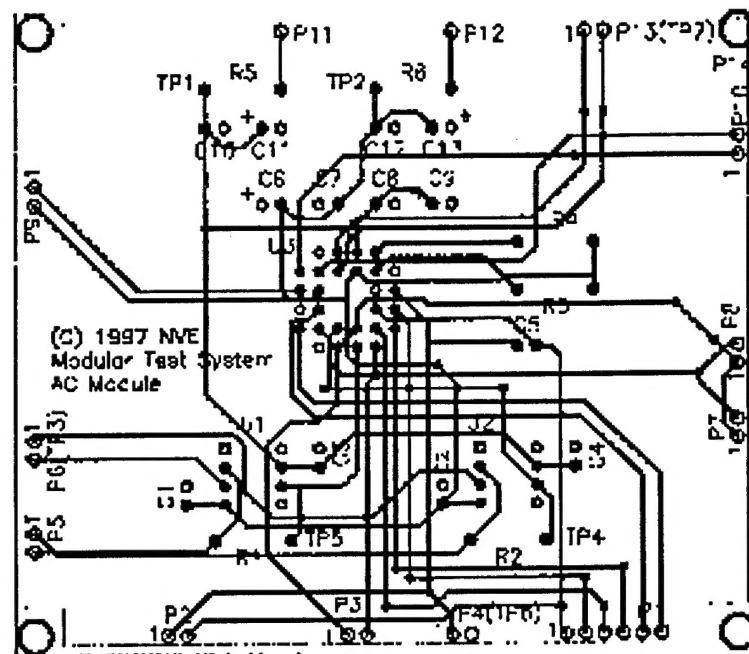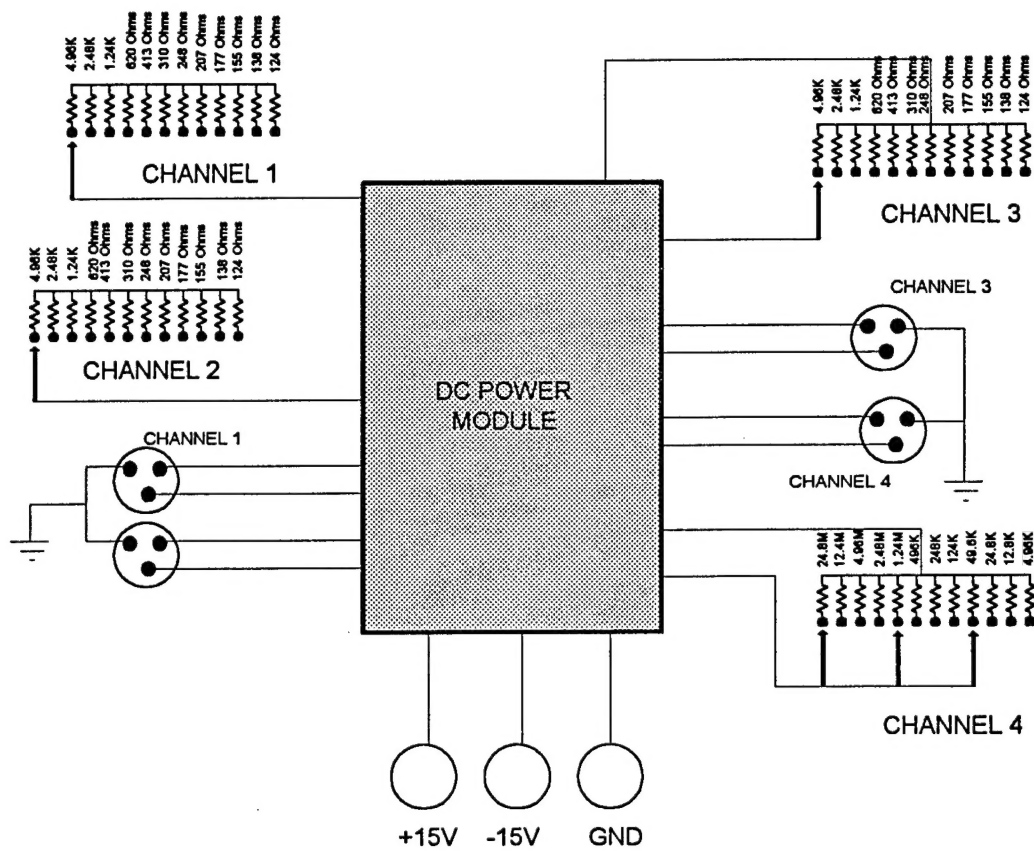
Figure 9: The actual AC module circuit is based on the AD698 modulator/demodulator chip.

DC POWER MODULE BLOCK DIAGRAM

Figure 10: The DC module is simply to provide a source of high precision, low noise currents for bridge excitation and biasing purposes.
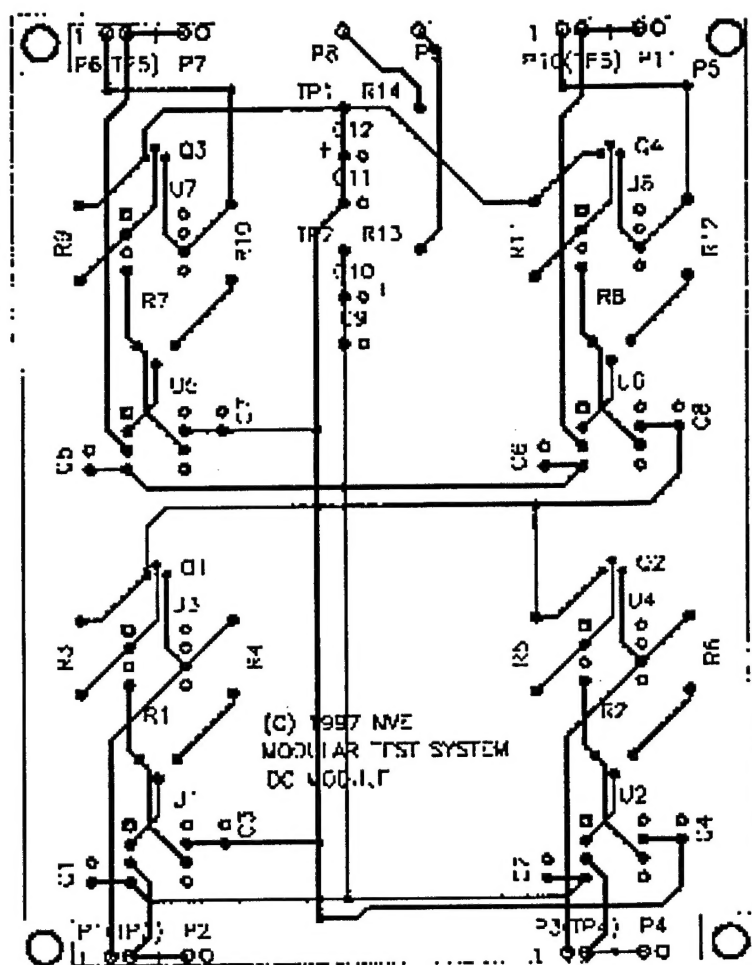
Figure 11: DC module circuit layout.

4) Full bridge fabrication

A full bridge of spin dependent tunnel arrays was fabricated with integrated biasing straps. This design was described extensively in the past two reports. We have learned a lot in the process of making these devices. In particular, the FeMn pinning layer creates many processing challenges. It is very chemically reactive. Enough so that any wet etch of the device will completely destroy an FeMn layer by undercutting the photoresist mask. As a result, we have developed a completely dry etch process. This is especially hard in light of the "wedding cake" structure of the device (the bottom electrode is larger than the top electrode). The top electrode is formed with an ion mill step which must cut deep enough to go through the entire top electrode thickness (~200Å) and then stop in the insulating barrier (~20Å). This kind of depth precision milling is presently achieved only through careful calculation and monitoring of the milling

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process. We are, however, developing a systematic method for this precision milling though the use of special test structures and procedures.
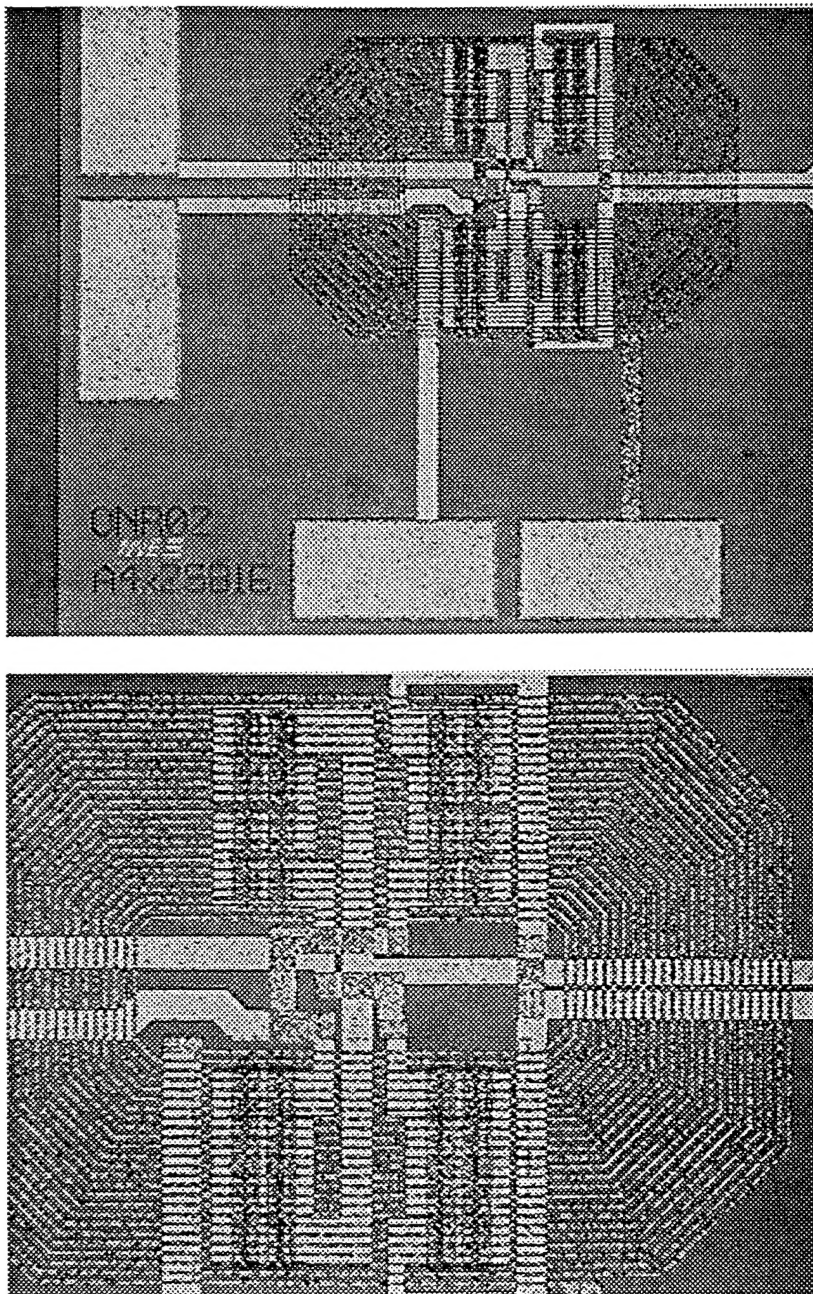

Figure 12: Close and far views of a full bridge with bias coils. The coil is the octagonal set of wires and the bridge elements are arrays of 16 SDT elements underneath the coils.